REMARKS

Claims 1-8 are pending in the application. Claims 5-8 have been withdrawn as being drawn to a non-elected invention. Claim 1 has been amended by the present amendment. The amendments are fully supported by the specification as originally filed.

Claim 1 was rejected under 35 USC 112, second paragraph, as being indefinite because of the phrase "preventing flash of a resin compound that forms the encapsulant on the exposed die pad and the inner leads due to the reduced spacing between the adjacent middle portions of the leads." Claim 1 has been amended to delete this language, thereby obviating the rejection.

Applicants' invention is directed to a semiconductor package for preventing resin flash. A lead frame is used as a chip carrier, the lead frame having a die pad and a plurality of leads surrounding the die pad. Each lead is defined into an inner lead, a middle portion, and an outer lead, where the middle portion includes protrusions formed on two sides, so as to reduce spacing between adjacent middle portions of the leads.

Applicants' claimed invention can provide significant benefits. By providing protrusions and reduced spacing between the middle portions, resin flow in a subsequent encapsulation process is slowed down in speed, thereby reducing the area available for resin flashes to occur and substantially eliminating the occurrence of resin flashes on the leads (see specification at page 7, first full paragraph). By eliminating resin flashes, die-bonding and wire-bonding processes can be performed smoothly, while assuring the quality and reliability of fabricated semiconductor packages.

Claims 1 and 2 were rejected under 35 USC 103(a) as being unpatentable over U.S. Patent 5,523,608 to Kitaoka et al. (hereinafter "Kitaoka") in view of U.S. Patent 6,315,465 to Mizue et al. (hereinafter "Mizue"). Claims 3 and 4 were rejected under 35 USC 103(a) as being unpatentable over Kitaoka in view of Mizue, and further in view of U.S. Patent 5,479,051 to Waki et al. (hereinafter "Waki"). These rejections are respectfully traversed.

As discussed in the Amendment filed on October 24, 2003, Kitaoka discloses a multi-chip semiconductor package incorporating a solid state image sensor and a peripheral IC, for reducing packaging area (see column 2, lines 14-17). But Kitaoka fails to teach or suggest middle portions of leads that extend outwardly to form protrusions (see Office Action, page 3), thereby preventing resin flashes by slowing resin flow due to a narrowed arrangement of middle portions of the leads.

Mizue fails to remedy the deficiencies of the Kitaoka reference. In the Office Action, FIG. 3 of Mizue was cited for teaching "middle portions" of leads extending "outwardly at sides thereof to form protrusions" (Office Action, page 3, last paragraph). However, one of ordinary skill in the art would not be motivated to combine the Mizue and Kitaoka references, at least for the reason that Mizue is structurally different from Kitaoka as to the locations of the die pad, leads, and encapsulant. For example, referring to FIGS. 2 and 3 of Mizue, the outward extending portion of each outer lead pin 10 is **not** encapsulated by encapsulating portion 18, as required in Applicants' claim 1.

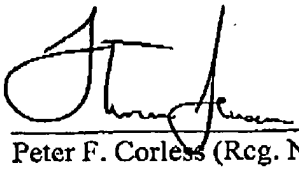
Therefore, one of ordinary skill in the art would not be motivated to combine the outward extending portion of the outer lead pin 10 in Mizue, which is not encapsulated, with the package disclosed in Kitaoka. The claimed reduction of spacing between adjacent leads which slows resin flow during molding is taught only in the Applicants' claimed invention, **not** in the Mizue or Kitaoka references.

Therefore, claim 1 is patentable over the combination of Kitaoka in view of Mizue. Claim 2, which depends from claim 1, also is patentable over these references. Moreover, the specific range of spacing recited in claim 2 is discussed on page 6, first paragraph of the specification, where the stated range allows resin flow to slow down in speed during molding, which reduces the area available for forming a resin flash, so as to prevent the occurrence of resin flashes.

The rejection of claims 3 and 4 is traversed for at least the reasons discussed above. Although the Waki reference was cited for teaching tapes adhered to the first and second sides of a lead frame, Waki still fails to remedy the deficiencies of the Kitaoka and Mizue references. Specifically, Waki fails to teach or suggest a plurality of leads having middle portions which extend outwardly to form protrusions for reducing spacing between adjacent middle portions. Therefore, even if Waki were combined with Kitaoka and Mizue, the combination would still fail to teach or suggest the Applicants' claimed semiconductor package that is capable of preventing resin flashes.

It is believed the application is in condition for immediate allowance, which action is earnestly solicited.

Respectfully submitted,



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